

CLAIMS

1. A data strobe circuit, comprising:

a first logic circuit coupled to receive a global data strobe signal and a first enable signal, the first logic circuit generating a first data strobe signal responsive to the global data strobe signal when the first enable signal is active;

a second logic circuit coupled to receive the global data strobe signal and a second enable signal, the second logic circuit generating a second data strobe signal responsive to the global data strobe signal when the second enable signal is active; and

a control circuit coupled to the first and second logic circuits, the control circuit receiving a write control signal, the control circuit being operable to generate an active first enable signal and to generate an active second enable signal responsive to receiving an active write control signal after generating the active first enable signal.

2. The data strobe circuit of claim 1 wherein the control circuit is operable to generate an inactive first enable signal when the active second enable signal is generated.

3. The data strobe circuit of claim 1 wherein the control circuit comprises:

a flip-flop being set or reset responsive to a transition of a signal applied to an control input of the flip-flop, the flip-flop having a first output coupled to an enable input of the first logic circuit and a second output coupled to an enable input of the second logic circuit, the first and second output being compliments of each other so that either the first logic circuit or the second logic circuit is enabled depending on whether the flip-flop is set or reset, respectively; and

a logic gate having an output coupled to the control input of the flip-flop, the logic gate receiving the first data strobe signal and the write control signal, the logic gate being enabled when the write control signal is active to allow the first data strobe signal to set or reset the flip-flop.

4. The data strobe circuit of claim 3 wherein the control input of the flip-flop comprises a clock input to the flip-flop so that a signal applied to the clock input sets or resets the flip-flop by toggling the flip-flop.

5. The data strobe circuit of claim 3 wherein the transition of the signal applied to the control input of the flip-flop sets the flip-flop, and wherein the data strobe circuit further comprises a logic gate having an output coupled to reset input of the flip-flop, the logic gate receiving the second data strobe signal to allow the second data strobe signal to reset the flip-flop.

6. The data strobe circuit of claim 1 wherein each of the first and second logic circuits further comprise a second enable input to enable or disable the first and second logic circuits, the second enable input of the first and second logic circuits being coupled to receive a data strobe write enable signal.

7. A data sampling circuit for sampling a data signal applied to a data terminal, the data sampling circuit comprising:

a plurality of data capture circuits each having a data input coupled to the data terminal, each of the data capture circuits further including a clock input coupled to receive a respective data strobe signal for sampling data applied to the data terminal responsive to the data strobe signal; and

a data strobe input circuit receiving a global data strobe signal and a write control signal, the data strobe input circuit being operable to generate successive data strobe signals applied to the clock inputs of successive ones of the data capture circuits responsive to the write control signal being active.

8. The data sampling circuit of claim 7 wherein the data capture circuits each comprise a flip-flop.

9. The data sampling circuit of claim 7 wherein the data strobe input circuit comprises:

a first logic circuit coupled to receive the global data strobe signal and a first enable signal, the first logic circuit generating first and second data strobe signals responsive to the global data strobe signal when the first enable signal is active, the first data strobe signal being applied to the clock input of a first of the data capture circuits and the second data strobe signal being applied to the clock input of a second of the data capture circuits;

a second logic circuit coupled to receive the global data strobe signal and a second enable signal, the second logic circuit generating third and fourth data strobe signals responsive to the global data strobe signal when the second enable signal is active, the third data strobe signal being applied to the clock input of a third of the data capture circuits and the fourth data strobe signal being applied to the clock input of a fourth of the data capture circuits; and

a control circuit coupled to the first and second logic circuits, the control circuit receiving the write control signal, the control circuit being operable to generate an active first enable signal responsive to receiving the active write control signal and to generate an active second enable signal after generating the active first enable signal.

10. The data sampling circuit of claim 9 wherein the control circuit is operable to generate an inactive first enable signal responsive to generating the active second enable signal.

11. The data sampling circuit of claim 9 wherein the control circuit comprises:

a flip-flop being set or reset responsive to a transition of a signal applied to an control input of the flip-flop, the flip-flop having a first output coupled to an enable input of the first logic circuit and a second output coupled to an enable input of the second logic circuit, the first and second output being compliments of each other so that either the first logic circuit or the second logic circuit is enabled depending on whether the flip-flop is set or reset, respectively; and

a logic gate having an output coupled to the control input of the flip-flop, the logic gate receiving the first data strobe signal and the write control signal, the logic gate being enabled when the write control signal is active to allow the first data strobe signal to set or reset the flip-flop.

12. The data sampling circuit of claim 11 wherein the control input of the flip-flop comprises a clock input to the flip-flop so that a signal applied to the clock input sets or resets the flip-flop by toggling the flip-flop.

13. The data sampling circuit of claim 11 wherein the transition of the signal applied to the control input of the flip-flop sets the flip-flop, and wherein the data strobe circuit further comprises a logic gate having an output coupled to reset input of the flip-flop, the logic gate receiving the second data strobe signal to allow the second data strobe signal to reset the flip-flop.

14. The data sampling circuit of claim 9 wherein each of the first and second logic circuits further comprise a second enable input to enable or disable the first and second logic circuits, the second enable input of the first and second logic circuits being coupled to receive a data strobe write enable signal.

15. The data sampling circuit of claim 7 wherein the first and second data strobe signals comprise the leading and trailing edges, respectively, of a first pulse generated responsive to the global data strobe signal, and the third and fourth data strobe signals comprise the leading and trailing edges, respectively, of a second pulse generated responsive to the global data strobe signal.

16. A memory device, comprising:
a row address circuit operable to receive row address signals applied to an external terminal and to decode the row address signals to provide a row address;

a column address circuit operable to receive column address signals applied to an external terminal and to decode the column address signals to provide a column address;

at least one array of memory cells operable to store data written to or read from the array at a location determined by the row address and the column address;

a data path circuit operable to couple data signals corresponding to the data between the at least one array and an external data terminal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to an external terminal; and

a data strobe circuit coupled to a component of the memory device, the data strobe circuit comprising:

a first logic circuit coupled to receive a global data strobe signal and a first enable signal, the first logic circuit generating a first data strobe signal responsive to the global data strobe signal when the first enable signal is active;

a second logic circuit coupled to receive the global data strobe signal and a second enable signal, the second logic circuit generating a second data strobe signal responsive to the global data strobe signal when the second enable signal is active; and

a control circuit coupled to the first and second logic circuits, the control circuit receiving a write control signal, the control circuit being operable to generate an active first enable signal and to generate an active second enable signal responsive to receiving an active write control signal after generating the active first enable signal.

17. The memory device of claim 16 wherein the data strobe circuit is coupled to the data path circuit so that the first and second data strobe signals can be used to sample write data coupled the external data terminal.

18. The memory device of claim 16 wherein the control circuit is operable to generate an inactive first enable signal when the active second enable signal is generated.

19. The memory device of claim 16 wherein the control circuit comprises:
a flip-flop being set or reset responsive to a transition of a signal applied to an control input of the flip-flop, the flip-flop having a first output coupled to an enable input of the first logic circuit and a second output coupled to an enable input of the second logic circuit, the first and second output being compliments of each other so that either the first logic circuit or the second logic circuit is enabled depending on whether the flip-flop is set or reset, respectively; and

a logic gate having an output coupled to the control input of the flip-flop, the logic gate receiving the first data strobe signal and the write control signal, the logic gate being enabled when the write control signal is active to allow the first data strobe signal to set or reset the flip-flop.

20. The memory device of claim 19 wherein the control input of the flip-flop comprises a clock input to the flip-flop so that a signal applied to the clock input sets or resets the flip-flop by toggling the flip-flop.

21. The memory device of claim 19 wherein the transition of the signal applied to the control input of the flip-flop sets the flip-flop, and wherein the data strobe circuit further comprises a logic gate having an output coupled to reset input of the flip-flop, the logic gate receiving the second data strobe signal to allow the second data strobe signal to reset the flip-flop.

22. The memory device of claim 16 wherein each of the first and second logic circuits further comprise a second enable input to enable or disable the first and second logic circuits, the second enable input of the first and second logic circuits being coupled to receive a data strobe write enable signal.

23. The memory device of claim 16 wherein the memory device comprises a dynamic random access memory device.

24. The memory device of claim 16 wherein the global data strobe signal is applied to an externally accessible terminal of the memory device.

25. A memory device operating in synchronism with a clock signal, comprising:

- a row address circuit operable to receive row address signals applied to an external terminal and to decode the row address signals to provide a row address;

- a column address circuit operable to receive column address signals applied to an external terminal and to decode the column address signals to provide a column address;

- at least one array of memory cells operable to store data written to or read from the array at a location determined by the row address and the column address;

- a data path circuit operable to couple data signals corresponding to the data between the at least one array and an external data terminal, the data path circuit including a write data path comprising:

- a plurality of data capture circuits each having a data input coupled to the external data terminal, each of the data capture circuits further including a clock input coupled to receive a respective data strobe signal for sampling data applied to the external data terminal responsive to the data strobe signal; and

- a data strobe input circuit receiving a global data strobe signal and a write control signal, the data strobe input circuit being operable to generate successive data strobe signals applied to the clock inputs of successive ones of the data capture circuits responsive to the write control signal being active; and

- a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to an external command terminal.

26. The memory device of claim 25 wherein the write control signal comprises a write signal generated a predetermined number of clock signal periods prior to internally writing data to the array of memory cells.

27. The memory device of claim 25 wherein the data capture circuits each comprise a flip-flop.

28. The memory device of claim 25 wherein the data strobe input circuit comprises:

a first logic circuit coupled to receive the global data strobe signal and a first enable signal, the first logic circuit generating first and second data strobe signals responsive to the global data strobe signal when the first enable signal is active, the first data strobe signal being applied to the clock input of a first of the data capture circuits and the second data strobe signal being applied to the clock input of a second of the data capture circuits;

a second logic circuit coupled to receive the global data strobe signal and a second enable signal, the second logic circuit generating third and fourth data strobe signals responsive to the global data strobe signal when the second enable signal is active, the third data strobe signal being applied to the clock input of a third of the data capture circuits and the fourth data strobe signal being applied to the clock input of a fourth of the data capture circuits; and

a control circuit coupled to the first and second logic circuits, the control circuit receiving the write control signal, the control circuit being operable to generate an active first enable signal responsive to receiving the active write control signal and to generate an active second enable signal after generating the active first enable signal.

29. The memory device of claim 28 wherein the control circuit is operable to generate an inactive first enable signal responsive to generating the active second enable signal.

30. The memory device of claim 28 wherein the control circuit comprises:

a flip-flop being set or reset responsive to a transition of a signal applied to an control input of the flip-flop, the flip-flop having a first output coupled to an enable input of the first logic circuit and a second output coupled to an enable input of the second logic circuit, the first and second output being compliments of each other so that either the first

logic circuit or the second logic circuit in enabled depending on whether the flip-flop is set or reset, respectively; and

a logic gate having an output coupled to the control input of the flip-flop, the logic gate receiving the first data strobe signal and the write control signal, the logic gate being enabled when the write control signal is active to allow the first data strobe signal to set or reset the flip-flop.

31. The memory device of claim 30 wherein the control input of the flip-flop comprises a clock input to the flip-flop so that a signal applied to the clock input sets or resets the flip-flop by toggling the flip-flop.

32. The memory device of claim 30 wherein the transition of the signal applied to the control input of the flip-flop sets the flip-flop, and wherein the data strobe circuit further comprises a logic gate having an output coupled to reset input of the flip-flop, the logic gate receiving the second data strobe signal to allow the second data strobe signal to reset the flip-flop.

33. The memory device of claim 28 wherein each of the first and second logic circuits further comprise a second enable input to enable or disable the first and second logic circuits, the second enable input of the first and second logic circuits being coupled to receive a data strobe write enable signal.

34. The memory device of claim 25 wherein the first and second data strobe signals comprise the leading and trailing edges, respectively, of a first pulse generated responsive to the global data strobe signal, and the third and fourth data strobe signals comprise the leading and trailing edges, respectively, of a second pulse generated responsive to the global data strobe signal.

35. The memory device of claim 25 wherein the synchronous memory device comprises a synchronous dynamic random access memory device.

36. The synchronous memory device of claim 25 wherein the global data strobe signal is applied to an externally accessible terminal of the memory device.

37. A computer system, comprising:
a processor having a processor bus;
an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;
an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and
a memory device coupled to the processor bus adapted to allow data to be stored, the memory device comprising:

a row address circuit operable to receive row address signals applied to an external terminal and to decode the row address signals to provide a row address;

a column address circuit operable to receive column address signals applied to an external terminal and to decode the column address signals to provide a column address;

at least one array of memory cells operable to store data written to or read from the array at a location determined by the row address and the column address;

a data path circuit operable to couple data signals corresponding to the data between the at least one array and an external data terminal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to an external terminal; and

a data strobe circuit coupled to a component of the memory device, the data strobe circuit comprising:

a first logic circuit coupled to receive a global data strobe signal and a first enable signal, the first logic circuit generating a first data strobe signal responsive to the global data strobe signal when the first enable signal is active;

a second logic circuit coupled to receive the global data strobe signal and a second enable signal, the second logic circuit generating a second data strobe signal responsive to the global data strobe signal when the second enable signal is active; and

a control circuit coupled to the first and second logic circuits, the control circuit receiving a write control signal, the control circuit being operable to generate an active first enable signal and to generate an active second enable signal responsive to receiving an active write control signal after generating the active first enable signal.

38. The computer system of claim 37 wherein the data strobe circuit is coupled to the data path circuit so that the first and second data strobe signals can be used to sample write data coupled the external data terminal.

39. The computer system of claim 37 wherein the control circuit is operable to generate an inactive first enable signal when the active second enable signal is generated.

40. The computer system of claim 37 wherein the control circuit comprises:

a flip-flop being set or reset responsive to a transition of a signal applied to an control input of the flip-flop, the flip-flop having a first output coupled to an enable input of the first logic circuit and a second output coupled to an enable input of the second logic circuit, the first and second output being compliments of each other so that either the first logic circuit or the second logic circuit is enabled depending on whether the flip-flop is set or reset, respectively; and

a logic gate having an output coupled to the control input of the flip-flop, the logic gate receiving the first data strobe signal and the write control signal, the logic gate being enabled when the write control signal is active to allow the first data strobe signal to set or reset the flip-flop.

41. The computer system of claim 40 wherein the control input of the flip-flop comprises a clock input to the flip-flop so that a signal applied to the clock input sets or resets the flip-flop by toggling the flip-flop.

42. The computer system of claim 40 wherein the transition of the signal applied to the control input of the flip-flop sets the flip-flop, and wherein the data strobe circuit further comprises a logic gate having an output coupled to reset input of the flip-flop, the logic gate receiving the second data strobe signal to allow the second data strobe signal to reset the flip-flop.

43. The computer system of claim 37 wherein each of the first and second logic circuits further comprise a second enable input to enable or disable the first and second logic circuits, the second enable input of the first and second logic circuits being coupled to receive a data strobe write enable signal.

44. The computer system of claim 37 wherein the memory device comprises a dynamic random access memory device.

45. The computer system of claim 37 wherein the memory device of claim 16 wherein the global data strobe signal is applied to an externally accessible terminal of the memory device.

46. A computer system, comprising:
a processor having a processor bus;
an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;
an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and
a synchronous memory device operating in synchronism with a clock signal, the synchronous memory device being coupled to the processor bus adapted to allow data to be stored, the synchronous memory device comprising:

a row address circuit operable to receive row address signals applied to an external terminal and to decode the row address signals to provide a row address;

a column address circuit operable to receive column address signals applied to an external terminal and to decode the column address signals to provide a column address;

at least one array of memory cells operable to store data written to or read from the array at a location determined by the row address and the column address;

a data path circuit operable to couple data signals corresponding to the data between the at least one array and an external data terminal, the data path circuit including a write data path comprising:

a plurality of data capture circuits each having a data input coupled to the external data terminal, each of the data capture circuits further including a clock input coupled to receive a respective data strobe signal for sampling data applied to the external data terminal responsive to the data strobe signal; and

a data strobe input circuit receiving a global data strobe signal and a write control signal, the data strobe input circuit being operable to generate successive data strobe signals applied to the clock inputs of successive ones of the data capture circuits responsive to the write control signal being active; and

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to an external command terminal.

47. The computer system of claim 46 wherein the write control signal comprises a write signal generated a predetermined number of clock signal periods prior to internally writing data to the array of memory cells.

48. The computer system of claim 46 wherein the data capture circuits each comprise a flip-flop.

49. The computer system of claim 46 wherein the data strobe input circuit comprises:

a first logic circuit coupled to receive the global data strobe signal and a first enable signal, the first logic circuit generating first and second data strobe signals responsive to the global data strobe signal when the first enable signal is active, the first data strobe signal being applied to the clock input of a first of the data capture circuits and the second data strobe signal being applied to the clock input of a second of the data capture circuits;

a second logic circuit coupled to receive the global data strobe signal and a second enable signal, the second logic circuit generating third and fourth data strobe signals responsive to the global data strobe signal when the second enable signal is active, the third data strobe signal being applied to the clock input of a third of the data capture circuits and the fourth data strobe signal being applied to the clock input of a fourth of the data capture circuits; and

a control circuit coupled to the first and second logic circuits, the control circuit receiving the write control signal, the control circuit being operable to generate an active first enable signal responsive to receiving the active write control signal and to generate an active second enable signal after generating the active first enable signal.

50. The computer system of claim 49 wherein the control circuit is operable to generate an inactive first enable signal responsive to generating the active second enable signal.

51. The computer system of claim 49 wherein the control circuit comprises:

a flip-flop being set or reset responsive to a transition of a signal applied to an control input of the flip-flop, the flip-flop having a first output coupled to an enable input of the first logic circuit and a second output coupled to an enable input of the second logic circuit, the first and second output being compliments of each other so that either the first logic circuit or the second logic circuit is enabled depending on whether the flip-flop is set or reset, respectively; and

a logic gate having an output coupled to the control input of the flip-flop, the logic gate receiving the first data strobe signal and the write control signal, the logic gate being enabled when the write control signal is active to allow the first data strobe signal to set or reset the flip-flop.

52. The computer system of claim 51 wherein the control input of the flip-flop comprises a clock input to the flip-flop so that a signal applied to the clock input sets or resets the flip-flop by toggling the flip-flop.

53. The computer system of claim 51 wherein the transition of the signal applied to the control input of the flip-flop sets the flip-flop, and wherein the data strobe circuit further comprises a logic gate having an output coupled to reset input of the flip-flop, the logic gate receiving the second data strobe signal to allow the second data strobe signal to reset the flip-flop.

54. The computer system of claim 49 wherein each of the first and second logic circuits further comprise a second enable input to enable or disable the first and second logic circuits, the second enable input of the first and second logic circuits being coupled to receive a data strobe write enable signal.

55. The computer system of claim 46 wherein the first and second data strobe signals comprise the leading and trailing edges, respectively, of a first pulse generated responsive to the global data strobe signal, and the third and fourth data strobe signals comprise the leading and trailing edges, respectively, of a second pulse generated responsive to the global data strobe signal.

56. The computer system of claim 43 wherein the synchronous memory device comprises a synchronous dynamic random access memory device.

57. The computer system of claim 46 wherein the global data strobe signal is applied to an externally accessible terminal of the memory device

58. A method of generating data strobe pulses responsive to global data strobe pulses, the method comprises:

generating a first data strobe pulse responsive to a first of the global data strobe pulses; and

generating a second data strobe pulse responsive to a second of the global data strobe pulses only if a write command is active.

59. The method of claim 58 wherein the act of generating a second data strobe pulse responsive to the second of the global data strobe pulses only if the first data strobe pulse was generated comprises:

determining if the first data strobe pulse was generated responsive to the first of the global data strobe pulses; and

if so, generating the second data strobe pulse responsive to the second of the global data strobe pulses.

60. A method of sampling a data signal responsive to a global data strobe pulse, the method comprises:

periodically sampling the data signal using a first storage device responsive to each of a plurality of global data strobe pulses; and

in the event a write command becomes active, discontinuing sampling the data signal using the first storage device responsive to the global data strobe pulses and sampling the data signal using a second storage device responsive to a respective global data strobe pulse.

61. A method of generating data strobe pulses responsive to global data strobe pulses present on a signal line on which noise pulses may be present in a preamble prior to the first of a global data strobe pulse, the method comprising:

generating a first data strobe pulse responsive to a first of the global data strobe pulses present on the signal line;

generating a second data strobe pulse responsive to a second of the global data strobe pulses present on the signal line; and

inhibiting either a first or a second data strobe pulse from being generated responsive to noise pulses present on the signal line during the preamble.

62. The method of claim 61 wherein the act of inhibiting either a first or a second data strobe pulse from being generated responsive to noise pulses present on the signal line comprises:

checking if a write control signal is present when the noise pulses are generated; and

if the write control signal is not present, preventing a second data strobe pulse from being generated responsive to the noise pulse.

63. The method of claim 61 wherein the act of inhibiting either a first or a second data strobe pulse from being generated responsive to noise pulses present on the signal line comprises:

checking if a write control signal is present;

as long as the write control signal is not present, generating a first data strobe pulse responsive to each pulse on the signal line including global data strobe pulses and noise pulses;

when the write control signal becomes present, discontinuing the first data strobe pulses from being generated responsive to each pulse on the signal line including global data strobe pulses and noise pulses; and

when the write control signal becomes present, generating the second data strobe pulse responsive to a global data strobe pulse.